AMENDMENTS TO THE SPECIFICATION

[0001] This application is a divisional of and claims priority to U.S. Application No. 09/860,031, filed on May 16, 2001, now issued as Patent No. 6,795,367, entitled "Layout Technique for Address Signal Lines in Decoders Including Stitched Blocks," which claims priority to U.S. Provisional Application Serial No. 60/204,371, filed on May 16, 2000, entitled "An Optimal Layout Technique for Row/Column Decoders to Reduce Number of Blocks," the entirety of which are incorporated herein by reference.

[0026] To provide more area for the stitching routing lines between generic decoder blocks, a smaller pitch may be applied to the decoder array than the pixel pitch. FIG. 6 illustrates a decoder array 600 for use in a sensor with a 9 μm pixel pitch, where the pitch of the decoder array is reduced to 8.75 μm. In a sensor including thirty-two generic blocks, this provides an additional 8 μm of additional silicon space in which to [[providing]] provide the routing lines. FIG. 7 illustrates a layout for the angled connection 602 between the decoder array and the pixel array in order to minimize the distance (y2-y1).